

ispLEVER Release Notes

Version 1.0

Technical Support Line: 1-800-LATTICE or (408) 826-6002 LEVER-RN v1.0.0

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ispLEVER 1.0

The ispLEVER[™] 1.0 software supports ispLSI[®](1000, 2000, 5000VE, and 8000), ispMACH[®] (4000B/C, 4A3, 4A5, 5000VG), MACH 4, MACH 4 Low Voltage, MACH 5, MACH 5/1, MACH 5 Low Voltage, GAL[®], ispGAL[®], and ispGDX[®] device families.

The following topics are discussed in this section:

- □ Licensing
- Product Information
- □ New Features and Enhancements
- □ Known Issues and Solutions

Supported Platforms

The ispLEVER 1.0 software supports Windows[®]XP, Windows 2000 (Workstation mode only). Windows NT, and Windows 98.

License Features

- □ LSC_BASE license feature supports all ispLSI, ispMACH, MACH, GAL, ispGAL, and ispGDX devices up to 768 macrocells.
- □ LSC_ADVANCED license feature supports all Lattice high-density CPLDs.

This ispLEVER 1.0 software provides Project Navigator, ABEL[®] Compiler, ABEL-HDL and schematic entry, gate-level timing and functional and timing simulation, timing analysis, debug tools, and our ispVM[™] System programming suite.

The ispLEVER 1.0 software comprises four products.

HDL Base

The ispLEVER HDL Base software includes ispLEVER, ispVM System; Mentor Graphics[®] ModelSim[®] and LeonardoSpectrumTM; and Synplicity[®] Synplify[®] (Base) tools.

HDL Advanced

The ispLEVER HDL Advanced software includes ispLEVER, ispVM System; Mentor Graphics ModelSim and Leonardo Spectrum; and Synplicity Synplify (Advanced) tools.

Exemplar Advanced

The ispLEVER Exemplar Advanced software includes ispLEVER, ispVM System, and Mentor Graphics (Advanced) tools.

Advanced System

The ispLEVER Advanced System software includes ispLEVER and ispVM System.

The following new features and enhancements are available in all the ispLEVER 1.0 software products:

- □ New Device Families Support
- □ Unified Design Flow for New and Legacy Devices
- □ New Style Project Navigator
- □ HTML Fitter Report Format
- Unified Constraint Editor
- □ ispEXPLORERTM
- □ ispUPDATETM
- New Version CAE Tools
- □ SVF File Generation
- Checksum as USERCODE Default
- Updates to ispVM Programming Software

New Device Families Support

This release supports the following new device families:

- □ SuperFast ispMACH 4000B/C
- □ SuperBig ispMACH 5000VG
- □ SuperWide ispLSI 5000VE

Unified Design Flow for New and Legacy Devices

The new ispLEVER software provides unified constraint flow and design environment for all Lattice devices, including new and legacy devices. The unified design flow provides fast, efficient runtime and competitive device performance and utilization.

Supported Legacy Devices

The following legacy devices are supported:

- GAL and ispGAL
- □ ispLSI 1000, 2000, and 8000 families
- □ MACH 4 and MACH 5, ispMACH 4A 3/5 families
- □ ispGDX

New Style Project Navigator

The standard Windows style is applied to the Project Navigator.

Collapse/Expand Tree View in Sources/Processes Window

The tree view control is used in both Sources and Processes windows of the Project Navigator (Figure 1). This allows you to collapse and expand the submodules in the design hierarchy tree or the subprocesses in the Processes window. You can select the vertical bar at the center of the window to adjust the sizes of the windows, and the setting will be saved after you exit the Project Navigator.

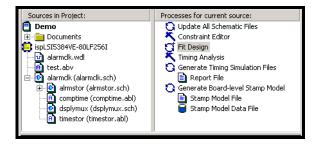


Figure 1. Tree View in Sources/Processes Window

New Output Panel with Report Viewer Embedded

The Output Panel is by default a docked window at the bottom of the Project Navigator. It displays the Automake log file, indicating errors and warnings. With the Report Viewer embedded in it, the Output Panel can display various report files on different tabs. You can choose to view report files in either the Output Panel or the Report Viewer.

To view report files in the Output Panel:

- 1. Choose **Options > Environment** to open the Environment Options dialog box.
- 2. On the Log tab, clear Using Report Viewer.

The Output Panel can be undocked or moved to a new position. Right-click in the Output Panel to display pop-up menus, which allow you to perform Copy, Clear, Print, and other common operations.

Context-Sensitive Pop-Up Menu

The Project Navigator provides a "context-sensitive" pop-up menu when you right-click on certain items in the Sources window, Processes window, or the Output Panel. The menus vary depending on where and when you click. Command definitions are available by pressing F1.

Single-Click to Start Processes

By default, processes are started by double-clicking the process in the Processes window. You can change this to a single click.

To start a process via a single click:

- 1. Choose **Options > Environment** to open the Environment Options dialog box.
- 2. On the General tab, select Single Click to Invoke Process.

Docked Toolbars

All the toolbars are by default attached to one edge of the Project Navigator window. You can dock a toolbar below the Project Navigator menu bar, or to the left, right, or bottom edge of the Project Navigator window.

To move a toolbar:

- 1. Click the move handle on a docked toolbar or click the title bar on a floating toolbar.
- 2. Drag the toolbar to a new location. If you drag the toolbar to the edge of the Project Navigator window, it becomes a docked toolbar.

New Tools Toolbar

The Tools toolbar (Figure 2) provides you with quick access to frequently used tools. You can toggle the display of this toolbar using the **View > Tools Toolbar** command.



Figure 2. Tools Toolbar

Tool Tip	Function
LeonardoSpectrum	Equivalent to Tools > LeonardoSpectrum Synthesis ; starts LeonardoSpectrum synthesis tool directly.
Synplify	Equivalent to Tools > Synplify Synthesis ; starts the Synplicity Synplify synthesis tool directly.
ModelSim	Equivalent to Tools > ModelSim Simulator ; starts the ModelSim Simulator directly.
ispEXPLORER	Equivalent to Tools > ispEXPLORER ; starts ispEXPLORER.

Enhanced Tools Menu

Some items on the Tools menu (Figure 3) have been enhanced with a graphic icon.



Figure 3. Enhanced Tools Menu

Select RTL Synthesis Dialog Box

The RTL Synthesis dialog box (Figure 4) allows you to select the synthesis tool for each project. You open this dialog box by choosing **Options > Select RTL Synthesis**. The synthesis tool you select is project-specific. For example, if you select the "LeonardoSpectrum" or "Synplicity" option for a project, this option will remain for this specific project.

The Select RTL Synthesis dialog box has been enhanced to include the **As Default** option. With this option checked, the tool you select in this dialog box will become the default synthesis tool for all your projects.



Figure 4. Select RTL Synthesis Dialog Box

HTML Fitter Report Format

A new HTML-based fitter report (Figure 5) makes report viewing fast and efficient through a standard Internet browser. Hyperlinks in the report allow you to quickly navigate signal paths for easy design debugging. When you run the HTML Fitter Report process, the report opens in your default Internet browser.

💥 prep_5.html - Netscape							
<u>File Edit View Go Communicator Help</u>							
Back Forward Reload Home	<i>2</i> Search	Metsca		🐌 Print Se	🛋 👔 ecurity Stop		N
🧯 🦋 Bookmarks 🦼 Location: file:///Cl/isp	TOOLS/i:	spcpld/ex	amples/	/verilog/pre	p_5/prep_5.html	💽 🚺	What's Related
Table of Contents	<u>Bid</u>	ir Si	.gna]	l List	<u>-</u>		•
• Top • Project Summary • Compilation Times • Design Summary	Bur		ligna	al Lis			
• Device Resource Summary		I א		C L Mc	P R R E C I F	Node Fanout	
• GLB Resource Summary • GLB Control Summary	Mc G	LB P	PTs		ESERP		Signal
Optimizer and Fitter Optic Pinout Listing	12 D 1 A	-		2 COM 5 COM		1D 2CD	
• Input Signal List • Output Signal List	6 B 1 C	7	25 3	5 COM 5 COM 7 COM		1 A I	V 118
• Bidir Signal List • Buried Signal List	1 C 12 B 3 D		9 2	7 COM 2 COM 4 COM		1 A 1 1 A 1 2 -BC- 1	<u>1 66</u>
• Signal Fanout List	3 D 19 C	0 6	3 . TO ,	4 COM 1 COM	*	_	<u>v 71 1</u> v 76

Figure 5. HTML Fitter Report

Unified Constraint Editor

The Constraint Editor (Figure 6) has a look similar to a Microsoft[®] Excel spreadsheet format. Flow sheets are incorporated at the bottom to facilitate an Engineering Design Flow Methodology.

🖻 🖬 🎒 🖪 🗠	\bigcirc	¥ 📋 I	Pro Loc Grp IO	Pwr Res	PLL HSI	Def 🢡 🎖	N?
D. prep1		Туре	Signal/Group Name 🛛 🛆	Group M	GLB	Macrocell	Pin
🕀 P Input Pins	1	Clock Input	CLK	N/A	G	0	2
P. Output Pins	2	Output	Q_0_	N/A		N/A	
pp dummy_0_ pp dummy_1_	3	Output	Q_1_	N/A		N/A	
pp_Q_0_	4	Output	Q_2_	N/A		N/A	-
	5	Output	Q_3_	N/A		N/A	
PP Q_2_	6	Output	Q_4_	N/A		N/A	
	7	Output	Q_5_	N/A		N/A	
	8	Output	Q_6_	N/A		N/A	
	9	Output	Q_7_	N/A		N/A	
pp Q_7_	10	Input	RST	N/A		N/A	
	11	Input	50	N/A		N/A	
	12	Input	51	N/A		N/A	
	13	Input	5_L	N/A		N/A	
	14	Input	d0_0_	N/A		N/A	
	Lin		L				

Figure 6. Constraint Editor Screen

The Constraint Editor reads the constraint file and displays the constraint settings. It lets you specify and modify pin and node location assignments, group assignments, I/O type settings, power level settings, resource reservations, PLL attributes, as well as output slew-rates and JEDEC file options. Modifications to the constraints can be made either through function dialog boxes or on the flow sheets.

Direct Constraints Editing

This new feature allows you to edit most constraints directly on the flow sheets without opening any dialog boxes. Editing constraints can be as simple as double-clicking a table cell and typing or selecting a desired constraint value. The constraint options on the pop-up menus also facilitate direct constraints editing.

When you edit directly, the Constraint Editor performs a simple check to ensure that your entry is applicable. For example, if you enter a pin number, the Constraint Editor checks to make sure the entry is applicable.

Auto-Increment and Auto-Decrement

You can auto-increment or auto-decrement pin, macrocell, GLB, and segment numbers in the Pin Attribute spreadsheet. Select a group of cells in the pin column, and right-click. In the popup menu, choose Pin Number to open the Enter a Pin Number dialog box (Figure 7). In the Enter a Pin Number dialog box, enter a pin number, and click **OK** to increment. Select the **Decrement Assignment** box to decrement, then click **OK**.

Enter a Pin Number		×										
Such as 1, 45, AK	1											
Pin Number												
	Decrement Assignment											
ОК	Cancel	<u>H</u> elp										

Figure 7. Enter a Pin Number Dialog Box

Pop-Up Menus

Various pop-up menus are available when you right-click in any sheet of the Constraint Editor. The menus enable you to edit constraint values, open dialog boxes, clear constraints, etc.

100 Step Undo/Redo

The **Undo** and **Redo** commands on the Edit menu allow you to reverse the edit process. **Undo** backs up one step each time you click the **Undo** command. You can reverse up to 100 steps from the time the constraint file was opened. **Redo** repeats the undone steps up to the point of the first Undo.

Enhanced Location Assignment Dialog Box

If you want to assign multiple signals to successive pins/macrocells at once, you can use the **Decrement Assignment** option to control the assignment order. This option is not visible until you have selected more than one signal in the Signals List.

Location Assignment					×
Signals List Bus Selection I I new_clk_time_0_ I new_clk_time_1_ I new_clk_time_2_ I new_clk_time_2_ I new_clk_time_3_ I new_clk_time_3_ I new_clk_time_1_ I new_clk_time_2_ I display_1_ I display_1_ I display_2_ I display_2_ I display_2_ I display_3_ I sound_altm Filter I nput I Output/Bidi		Assignment Pin A5 1/0 A2 1/0 A3 1/0 A4 1/0 A5 1/0 A4 1/0 A5 CLK A7 1/0 A8 CLK A7 1/0 A8 C Pin C Macrocc C GLB C Segment	Segme	×	
Existing Location Assignment List			🔽 Decre	ment Assignmer	ų.
Type 🛆 🛛 Signal Name	Segment G	LB	Macrocell	Pin	
Add Delete N	Modify Undo Ma				

Figure 8. Enhanced Location Assignment Dialog Box

As shown in Figure 8, if **Decrement Assignment** is cleared, the Constraint Editor assigns the first selected signal (display_0_) to the highlighted pin/macrocell (A5) and then successively assigns the other selected signals to the pins/macrocells following the highlighted pin/macrocell (display_1_ to A6; display_2_ to A7; display_3_ to A8). Checking **Decrement Assignment** also assigns the first selected signal (display_0_) to the highlighted pin/macrocell (A5), but the other selected signals are successively assigned to the pins/macrocells listed prior to the highlighted pin/macrocell (display_1_ to A4; display_2_ to A3; display_3_ to A2).

Enhanced Group Assignment Dialog Box

The Group Assignment Dialog Box (Figure 9) has been enhanced to include the **Keep Order** option as well as the **1** (Move Up) and **1** (Move Down) buttons. Use the two buttons to control signal order in a group. You can then check **Keep Order** to make the specified signal order take effect during the fitting process.

The new **Filter** button works with the four check boxes to improve the filter function. You can type text or wildcards in the text box and then click **Filter** to further filter the signals displayed in the Available Signals list.

Group Assignment			×
Group Assignment Assign Signals to Group Group Name Available Signals I I new_clk_time_0 I I new_clk_time_1 I I new_clk_time_2 I I new_clk_time_3	Selected Signals selected Signals new_alm_time_0_ new_alm_time_1_ new_alm_time_3_	V Keep Order	Assign Group to GLB Any C C D E F G Segment
Filter for Available Signals	idi 🗖 Buried Node	C Group	Not Available
Existing Group Assignment List		[a: 1	
Group Na 🛆 Keep Order	Segment GLB	Signals	
Add Delete	Modify Undo Modify	OK Canc	el Help

Figure 9. Enhanced Group Assignment Dialog Box

Enhanced Default Setting Dialog Box

The Default Setting dialog box (Figure 10) has been improved to display two columns. The left column displays constraint names. When you click a constraint name, its available values are shown in the right column. The constraint names and values listed in the two columns are device-dependent.

NOTE For ispMACH 4A3, MACH 4A5, MACH 4, MACH 4LV, MACH 5, MACH 5/1, and MACH 5 LV devices, the parametric Pullup settings are also set in the dialog box. By definition, the Default Setting parameters apply for the whole device. Signal specific settings are applied via the Pin Attribute spreadsheet.

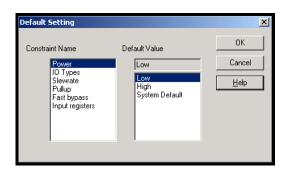


Figure 10. Default Setting Dialog Box

Assign Power Level for All Signals in a GLB

For ispMACH4A3/4A5 and MACH4/MACH5 device families, you can use the Assign Power Level dialog box (Figure 11) to apply a power level to a certain GLB. All signals in that GLB will then be set to that power level.

Assign Power Level (Default :	High)	×
Set Default power level : High	Assign power level : High	
Default power level for GLB	Assign power level for GLB	
04 08 0C 0D 1C 1D	1A 1B >>> <<	
Default OK	Cancel <u>H</u> elp	

Figure 11. Assign Power Level Dialog Box

Customize Colors

In the Set Colors dialog box (Figure 12), you can select colors to be displayed in the Constraint Editor sheets and the Package View main window.

Set Colors				×
Colors for Grid Text Color Fixed Text Color Grid Color	Automatic 💌	Text Back Color Fixed Text Back Color Grid Back Color	Automatic V	OK Cancel Apply
Colors for Package Unused Pin Color Input Pin Color IO Pin Color		System Pin Color Output Pin Color Reserved Pin Color	Automatic Automatic Automatic Automatic	<u>(U</u> se Default) <u>H</u> elp
Colors for Constrain		Color for Error Values	Red 💌	

Figure 12. Set Colors Dialog Box

Package View

The Constraint Editor Package View window (Figure 13) shows the actual pin assignments in the selected package. By default, the system (non-user) pins are highlighted in gray; reserved pins are in lime; assigned input pins are in blue; output pins in yellow and bi-directional pins in magenta. Unused pins are blank. You can also change these system default colors by choosing **Edit > Set Colors**. You can view this window by choosing **Device > Package View** from the Constraint Editor.

📴 Constraint Editor																	
Eile Edit Yiew Iools Window Help																	
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€ < 																	
Package View ispL5I5384VE-165LF256 : C:\ispTOOL5\ispcpId\examples\vhdl\compare																	
				isp	LSI5	5384	VE-1	65L	F250	6 (Bo	ottor	n Vie	w)				4
						1	1							1			-
	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	
	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	В4	В3	B2	B1	
	C16	C1E	C14	C13	C12	C11	C10	C9	C8	C7	Cfi	C5	C4	C3	C2	C1	
		U15	014	C13		UII	CIU	Ca.	0	07	CB	5	64	5	62		
	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	

Figure 13. Constraint Editor Package View

Drag and Drop Pin Assignments

The Package View provides a drag and drop feature for making pin assignments. You can drag signals from the signal tree of the Constraint Editor to the Package View window. You can also drag and drop signals inside the Package View window, as shown in Figure 14.

Cor	istrain	t Edito	or														
<u>File</u>	dit <u>P</u> ir	n Attrib	oute [evice	⊻iew	<u>₩</u> indo	w <u>H</u> el	р									
2		5	Q,	5	α	*	Ċ,	ric I	Loc Grp	IO Pwr Res PLL HSI Def	8	? N ?					
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📕 Pa								T		C:\ispTOOLS\ispcpld\examples	\vh	dl\comp	are\compare.lct*			_	
isp	LSI5	384	VE-1	165L	F25	6 (Be	ottom	ı Vie	w) 🔺	-D. top_schematic		Туре	Signal/Group Name ∇	Group Members	GLB	Macrocell	Pin
						•			· 🔳	P. Input Pins	1	Input	COMPDAT_1_	N/A		N/A	A13
	416	A1E	414	412	419	411	A10	A9	A8								
	AID	AIS	AI4	AIJ	ALZ	ALL	AIU	A9	Að								
	D10	D1F	D14	D12	D10	D11	B10	B9	B8	COMPDAT_1_@ A13 Dep COMPDAT_2							
	010	013	014	БГЗ	DIZ	ын	BIU	03	DO	pp COMPDAT_2_							
	C16	C15	C14	C13	C12	C11	C10	C9	CB	- pp DAT 0							
	010	013	014	013	012	CIT	010	03	00	-pp DAT_1_							
	D16	D15	D14	D13	D12	D11	D10	D9	D8	-pp DAT_2_							
	010	013	014	013	DIE	UII	DIO	03	00	-pp DAT_3_							
	F16	E15	E14	E13	F12	E11	E10	E9	E8	- pp RST							
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	F16	E15	F14	F13	F12	F11	F10	F9	F8	P. Output Pins							
					1	1	1.10			i M. Nets	1	-					•
4											•	▶ _\ Pin /	Attributes 🖌 Global 🤇	Constraints እ R	esou	rce Resen	/ation /

Figure 14. Drag and Drop Pin Assignments in Package View

You can drag and drop the input, output, or bidir signals from the signal list tree on the left side of the Pin Attribute sheet into the Package View package pins. When you select an assigned package pin, the associated signal in the Pin Attribute sheet will be highlighted.

Edit Pins

You can edit pins in the Package View, as shown in Figure 15, by right-clicking on the pin and selecting the **Unlock**, **Reserve**, **Un-reserve**, **Disable**, or **Locate** command in the pop-up menu. You can unlock assigned pins in the Package View.

🔤 Co	nstrain	t Edit	or													
File B	Edit Vi	ew T	ools \	Vindow	Help											
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isc	LSI5	384	VE-	165L	F250	6 (Bo	ottom	ı Vie	w) 🔺	⊡-D., top_schematic	Туре	Signal/Group N	Group Memb	GLB	Macrocell	Pin
						. (··· , 🔳	-P. Input Pins	1 Input	COMPDAT_1_	N/A		N/A	A13
	A16	A15	A14	A1 3	A12 COMF	A11 DAT 1	A10	A9 ked to r	A8 bin A13							
	B16	B15	B14	B13	Unic	_		B9	B8	COMPDAT_1_@A13						
	C16	C15	C14	C13		reserve		C9	C8							
	D16	D15	D14	D13	Loca Pin I	ate Propert	→	D9	D8							
	E16	E15	E14	E13	E12	E11	E10	E9	E8							
	F16	F15	F14	F13	F12	F11	F10	F9	F8 🔪	₽. Output Pins ₽. Nets	•					Þ
•											I ► Pin	Attributes & Glob	al Constraints λ	Reso	urce Resei	rvation

Figure 15. Edit Pin in Package View

Translating Mappable ispLSI and MACH Legacy Constraints

The new ispLEVER software gives you an improved and more unified constraint flow. You must convert legacy ispDesignEXPERT 8.2, 8.3, or 8.4 constraint files to ispLEVER constraint files before running your design in ispLEVER. To convert the constraint files, you can use the Legacy Constraints Translator by double-clicking on the Legacy Constraints Translator icon **F** in the Lattice Semiconductor program menu, or you can use the legacy2lci command line utility provided with the ispLEVER software, located in <install_path>\ispcpld\bin.

NOTE	Designs created in Lattice software older than ispDesignEXPERT 8.x
	must first be opened in ispDesignEXPERT 8.x, and then saved as an
	ispDesignEXPERT 8.x project.

MACH Devices

For MACH4 and MACH5 designs created with ispDesignEXPERT 8.2, 8.3, or 8.4 use a .vci constraint file, which must be converted to an .lci constraint file for ispLEVER.

ispLSI Devices

For ispLSI 1000, 2000, and 8000 family devices, designs created with ispDesignEXPERT 8.2, 8.3, or 8.4 use a Parameter File (.par), a Property File (.prp), a Pin File (.ppn), a User Code File (.ues), a Pin Reservation File (.rsp), or a Fitting Options Setting File (.xct), all of which can be converted to a single LCI file for ispLEVER. For details on constraint mapping, see "ispLSI Legacy Constraints Support" on page 22.

NOTES	 Because the design flow is changed from ispDesignEXPERT 8.x to ispLEVER 1.0 for ABEL designs, some of the internal signal labels may not match. Node constraints such as Regtype, Preserve, Protect and ECP might not convert properly to ispLEVER 1.0. Before beginning the conversion process, be sure to save an archive copy of your entire project directory.
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Converting Files Using the Legacy Constraints Translator

The Legacy Constraints Translator (Figure 16) is a graphical user interface application that reads the <projectName>.syn file, and other files according to the optional parameters.

Family:	Device	-	Device:	32EA	v
Part Nam ispLSI10	e: 32EA-125LT10	0	, .]
Option-	SI GAL\veril	alconshift e	dif.org		Ok
PPN		\conshif\cons	shif.ppn		Cancel
□ XCT □ UES					Apply
🔽 RSP	I_GAL\verilog	g\conshif\con	shif.rsp		Help
Message					ples\ispLSI_GAL

Figure 16. Legacy Constraints Translator

To convert files using the Legacy Constraints Translator:

- 1. Archive your project directory so that you will have a backup.
- 2. From the Lattice program menu, select **Legacy Constraints Translator** to open the program.
- 3. In the dialog, do the following:
 - a. In Project Name, select the ispDesignEXPERT 8.x project that you want to convert.
 - b. Under Select Device, the default is the current target device. If the target device is not supported, all options are disabled. To select a different device, you must change the project name in the Project Name field.
 - c. Under Options, select the files that you want to convert.

NOTE For ispLSI devices, all options are available for file extension selection. For MACH devices, not all options are available for selection.

4. Click **OK**. The selected legacy files are converted to ispLEVER files in the specified project directory, and the application exits. If you click **Apply** before clicking **OK**, you can re-select various options to convert, and stay in the application until you click **OK** to execute and exit.

Converting Files Using the legacy2lci Command Line Application

The utility "legacy2lci" reads all the ispDesignEXPERT 8.x project and constraint files (.syn, .vci, .prp, .par, .ppn, and .rsp) to create the ispLEVER 1.0 constraint file (.lci). Once the LCI constraint file is successfully created, you can load the Project File (.syn) from the ispLEVER Project Navigator. Note that if you did not run the legacy2lci utility to create the LCI file prior to opening the SYN file, the ispLEVER Project Navigator will automatically generate a "blank" LCI file with the defaulted device.

To translate design constraint files from 8.x into ispLEVER:

- 1. Archive your project directory so that you will have a backup.
- 2. For MACH4 or MACH5 devices, using the Windows Command Prompt, change directory (cd) to your project directory, and type (on one line):

```
<install_path>\ispcpld\bin\legacy2lci <project_name>
```

3. For ispLSI 1000 and 2000 devices, using the Windows Command Prompt, change directory (cd) to your project directory, and type (on one line):

```
<install_path>\ispcpld\bin\legacy2lci <project_name>
[-prp <filename_ext>]
[-p [-par <filename_ext>]]
[-n [-ppn <filename_ext>]]
[-u [-ues <filename_ext>]]
[-r [-rsp <filename_ext>]]
[-x [-xct <filename_ext>]]
[-ppnOnly <filename_ext>]
```

where [] denotes optional parameters for 1000 and 2000 devices:

-prp converts a user property file name that differs from the project name, <project_name>.prp. It is recommended that you not use the 8.4 system created _edif.prp. However, you can use the _edif.prp file in those cases where the <project_name>.prp file is 0 bytes or empty.

-p converts the PAR file. By default, the PAR file is <project_name>.par. When you use the -p option, the Part Name, PRP, and PPN defined in the PAR file are ignored.

-par is used to specify a PAR file name that differs from the project name, <project_name>.par.

-n converts the PPN file. By default the PPN file is <project_name>.ppn. When you use the -n option, the pin assignments in the PPN file are used, and those defined in the PRP file are ignored.

-ppn is used to specify a PPN file name that differs from the project name, <project_name>.ppn.

-u converts a UES file.

-ues is used to specify a UES file name that differs from the project name, <project_name>.ues.

-r converts an RSP file.

-rsp is used to specify an RSP file name that differs from the project name, <project_name>.rsp.

-x is used to specify an XCT file name that differs from the project name, <project_name>.xct

-ppnOnly is used to override all of the above parameters. When using ppnOnly, legacy2lci does not need a PRP and SYN file. The part name is derived from the PPN itself.

NOTES	• The ppnOnly option is case-sensitive. You must type the ppnOnly option exactly as shown.
	• For ispLSI 1000 and 2000 devices, the part name defined in <project_name>.syn will be used; therefore, the part name defined</project_name>
	in PAR file will be ignored.

- 4. After the conversion process, make sure that the converted LCI file is in your working project directory.
- 5. In ispLEVER, choose **File > Open** to open your Project File (.syn).

NOTES	• After you translate mappable constraints using the legacy2lci utility, you must resynthesize your design with your ispLEVER synthesis tool. You cannot import legacy EDIF files that were synthesized in ispDesignEXPERT 8.x directly into ispLEVER.
	• For legacy schematic designs, you may need to map old library symbols to equivalent new library symbols in ispLEVER after using the legacy2lci utility. Contact Lattice Technical Support for help with mapping old library schematic symbols with new library schematic symbols.

ispLSI Legacy Constraints Support

The tables on the following pages list the ispLSI legacy constraints support in the new release.

Family ispLSI Legacy	ispDesignEXPERT Device Constraints	ispDesignEXPERT Constraint Value	Description	ispLEVER Unified Device Constraints	ispLEVER Constraint Value	Constraint Type
Global G	Constraints					
1K/2K	ISP	ON, OFF	Prevents the use of all ISP pins	ISP	ON, OFF Default = ON	Global
1K/2K	ISP_EXCEPT_Y2	ON, OFF	Prevents the use of all ISP pins except the Y2 pin	ISP_EXCEPT_Y2	ON, OFF Default = OFF	Global
5K	TOE_AS_RESET	ON, OFF	Use TOE/IO0 as TOE or IO	TOE_AS_IO	ON, OFF Default = OFF	Global
1K/2K	Y1_AS_RESET	ON, OFF	Use Y1/RESET as Y1 or RESET	Y1_AS_RESET	ON, OFF Default = ON	Global
5K/8K	XOR	ON, OFF	Preserves all user 2- input XOR	KEEP_XOR	ON, OFF Default = ON	Global
5K/8K	LOWPOWER	ON, OFF	Turns on/off the turbo fuses	POWER	Low, MedLow, medHigh, High Default = High	Global
2K/5K/8K	OPENDRAIN	ON, OFF	Open drain feature	OPENDRAIN	ON, OFF Default = OFF	Global
5K	OUTDELAY	ON, OFF	Output delay feature	OUTDELAY	ON, OFF Default = OFF	Global
1K/2K/5K /8K	PULL	UP, HOLD, OFF	Pull up feature	PULLUP	OFF, UP, DOWN,HOLD Default is set by user	Global
1K/2K/5K /8K	SLOWSLEW	ON, OFF	Slew rate feature	SLEWRATE	SLOW, FAST Default = FAST	Global
5K	VOLTAGE	VCC, VCCIO	3.3 or 2.5 Voltage	VOLTAGE	VCC, VCCIO Default =VCCIO	Global
1K/2K/5K /8K	SECURITY	ON, OFF	Set G field of JEDEC	SECURITY	ON, OFF Default = OFF	Global
			User	USERCODE	STRING	Global
1K/2K/5K /8K	UES	String	Electronic Signature	USERCODE_FORM AT	HEX, BIN, ASCII Default = HEX	

Local Co	onstraints					
1K/2K/5K /8K	CLK	CLK0,CLK1,CLK2, CLK3, IOCLK0,IOCLK1, FASTCLK, SLOWCLK	Clock Assignment	CLK	CLK0,CLK1,CL K2, CLK3, IOCLK0,IOCLK 1, FASTCLK, SLOWCLK Default = None	Net
	PRESERVE	N/A	Prevents removal of a net	PRESERVE	Signal_list Default = None	Net
	SCP/ECP	Path Name	Start/End critical path	PTSABYPASS	Signal_list Default = None	Net
	PROTECT	N/A	Keeps the primitive	PROTECT	Signal_list Default = None	Symbol
	RESERVE_PIN	Pin Name	Prevents routing of signals to specified pin	Pin	Pin_number	Symbol
	PULL	UP, HOLD, OFF	Pull up feature	PULLUP	OFF, UP, DOWN,HOLD Default is set by user	External Pin
1K/2K	GROUP	Group Name	Group to GLB	Not supported		Net
	SAP/EAP	Path Name	Asynchronous path	Not supported		Net
	SNP/ENP	Path Name	No minimize path	Not supported		Net
	LXOR	N/A	Uses the device 2-input XOR	Not supported		Symbol
	OPTIMIZE	ON, OFF	Optimizes hard macro	Not supported		Symbol
	CRIT	N/A	Use ORP bypass	OSM BYPASS	Signal_list Default = None	External Pin
2K/5K/8K	SLOWSLEW	ON, OFF	Slew rate feature	SLEWRATE	FAST = Signal_List SLOW= Signal_List Default set by Global constraint	External Pin
2K/5K/8K	OPENDRAIN	ON, OFF	Open drain feature	IO TYPES	LVCMOS25_OD LVCMOS33_OD	External Pin
5K/8K	XOR	ON, OFF	Preserves Users XOR gate	KEEP_XOR	ON = signal list; OFF = signal list; Default set by Global constraint	Net
	SLP/ELP	Path Name	Low Power Path	POWER	Low = Signal_list medLow = Signal_list medHigh = Signal_list High = Signal_list Default set by Global constraint	Net

	STP/ETP	Path Name	Turbo (SPEED) Path	POWER	Low = Signal_list medLow = Signal_list medHigh = Signal_list High = Signal_list Default set by Global constraint	Net
1K/8K	REGTYPE	GLB, EITHER, IOC	Register Placement	Not supported		Symbol
8K	BFM	BFM Index	Node Placement	Not supported		Net
	LOCK_BFM	BFM Index	Group Pin Locking	Not supported		External Pin
	LOCK_GRP	GRP Index	Group Pin Locking	Not supported		External Pin

ispEXPLORER

The ispEXPLORER (Figure 17) lets you run multiple passes of your design using different combinations of Fitter/Optimizer settings and critical timing constraints to achieve the best solution. Results are summarized in a single spreadsheet and detailed reports for each run are accessible. The ispEXPLORER supports ispMACH 4000B/C, ispMACH 5000VG, and ispMACH 5000VE devices only.

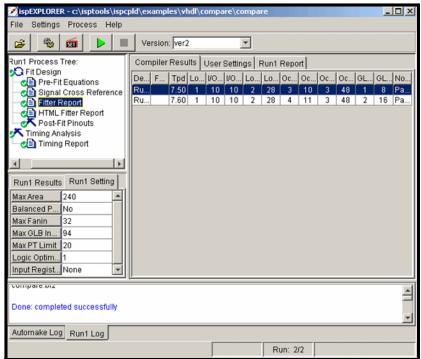


Figure 17. ispEXPLORER

The ispEXPLORER software helps you select the best constraint settings for your design by letting you run the design repeatedly with varied settings. The software gives you a single spreadsheet summary of results and settings after completion, making it easy to compare one group of settings with another. You can export the spreadsheet data into a Comma Delimited File (.csv) that you can import into a Microsoft Excel spreadsheet.

Use Predefined or Customized Settings

You can create a single run or multiple runs using different combinations of settings. When you accept the settings for the predefined files, which is the initial default setting, the software automatically creates a run for each of the .lci files using the predetermined settings. When you use customized settings, you can change each of the values. You can also select multiple values for each setting and have the software keep running the design until it has exhausted all possible combinations among the selected values or until it has reached a specified run stop threshold.

The predefined files are specially designed to give you the best Fmax or Tpd performance for the selected device.

Create Multiple Versions of Design Runs

You can create multiple versions with different runs. Each time you click the Start button, you have the choice of creating a new version or overwriting an existing version. When you create a new version, the software creates a new version directory inside your project folder and copies the design files into this directory. It generates new constraint files based on the current project constraint file, plus the new settings you select, and runs the design using these settings. The results and settings for each run are then saved in subdirectories of the new version directory.

Save the Best Constraints For Your Project

After experimenting with different settings to determine which constraint settings are best for your design, you can save the constraints by using the Save Setting pop-up command for a specific run. When you save these constraints in ispEXPLORER, the software updates your project, replacing only the constraints that you have changed; it does not replace the .lci files.

Configuring Run Settings

You can configure a run setting or condition that will stop is pEXPLORER when your condition is met. For example, you can set is pEXPLORER to stop when Fmax >= 100MHz.

Reading Previous ispEXPLORER Runs

You can review previous runs of ispEXPLORER by opening the .epl file.

ispUPDATE

The new ispUPDATE feature allows you to easily set up a proxy server to query the Lattice website for new software updates, device support, and enhancements. You can download patches and update files directly to your computer's disk drive.

The ispUPDATE program lets you select the software version to be updated when there are multiple versions of the software installed on the same computer. You can start the standalone ispUPDATE from the Lattice program menu (Figure 18).



Figure 18. Lattice Program Menu

For more details about ispUPDATE, refer to the Help Introduction section.

New Version CAE Tools

The synthesis, RTL and timing simulation tools integrated in the ispLEVER have been upgraded to new versions.

- □ Synplicity Synplify: from v6.2.2 to v7.0.2A
- □ Mentor Graphics LeonardoSpectrum: from v1999.1j to v2002a.13_OEM_Lattice
- □ Mentor Graphics ModelSim: from v5.4e to v5.5e_p1

SVF File Generation

The ispLEVER installation program allows you to set the software to automatically generate Serial Vector Format (.svf) files. The three SVF files generated are:

- SVF_ERASE_PROGRAM_VERIFY (<project>_epv.svf).
 Svf_erase_program_verify specifies erase, program, and verify operations for the SVF file.
- SVF_ERASE_PROGRAM_VERIFY_SECURE (<project>_epvs.svf).
 Svf_erase_program_verify_secure specifies erase, program, verify, and secure operations for the SVF file.
- □ SVF_VERIFY_ONLY (<project>_v.svf). Svf_verify_only specifies verify only operation for the SVF file.

See the *ispLEVER Installation Notice* for details on how to set the software to automatically generate Serial Vector Format (.svf) files as a global setting.

If you do not set ispLEVER to generate SVF files during software installation, you can manually set the options as a local setting in the Constraint Editor.

To manually set SVF file generation options:

- 1. In the Constraint Editor, click the Global Constraints Tab.
- In the SVF_ERASE_PROGRAM_VERIFY, SVF_ERASE_PROGRAM_VERIFY_SECURE, and SVF_VERIFY_ONLY columns, select ON in the menu. The default of these three options is OFF.

Checksum as USERCODE Default

The ispLEVER installation program allows you to set Checksum as the USERCODE default as global settings. See the *ispLEVER 1.0 Installation Notice* for details on how to set Checksum as the USERCODE default.

If you do not set ispLEVER to set Checksum as the USERCODE default during software installation, you can manually set the option as a local setting in the Constraint Editor.

To manually set Checksum as the USERCODE default:

- 1. In the Constraint Editor, click the Global Constraints Tab.
- 2. In the Usercode_format column, select CHECKSUM in the menu. The default is OFF.

NOTE CHECKSUM option is not available for MACH 4 and MACH 5 devices.

Updates to ispVM Programming Software

The ispVM programming software version 10.0.1A has new features, new device support, and software updates.

New Features

Added SVF Writer command line program (svf.exe) to support the ispLEVER software SVF file creation.

New Device Support

The ispVM programming software version 10.0.1A has added support for ispMACH 5768VG device.

Software Updates

□ The ispVM software version 10.0.1A has fixed "Read and Save JEDEC" and "Verify Only" operations for all MACH4A devices to prevent I/O glitching during "Read and Save" and Verify Only" operations. This is done by performing verification of the IDCODE followed by issuing a Bypass instruction to the device. Next, the UESRCODE of the device is read or verified depending on the operation. Finally, the device is enabled into programming mode to read or verify the device. When this is done, the I/O of the MACH4A will remain in HIZ during the entire "Read and Save" or "Verify Only" operations.

- □ The ispVM programming software version 10.0.1A has updated I/O BSCAN Vector Editor to support new package types.
- □ The ispVM programming software version 10.0.1A has updated ispVM command line support to return correct error codes.
- □ The ispVM programming software version 10.0.1A has write TDI(0) after HRD, TDR, HIR, AND TIR 0 in the SVF File.

The following known issues have been identified and their solutions are determined:

Legacy Constraints Conversions/Design Migration/Unified Constraint Editor Issues

Issue:	You cannot mix Exemplar and Synplicity .ppn conversions. If you convert a Synplicity PPN file, the bus nomenclature uses a [] to enclose the components of the bus (i.e $a[10]$). The Exemplar PPN files uses the () to enclose the components of the bus (i.e $a(10)$).
Solution:	Don't mix constraint files (.lci) that were created using different synthesis tools.
Devices Affected:	ispLSI 1000, 2000, and 8000
Issue:	If you don't import source constraints, PLL will not be recognized by the fitter.
Solution:	When using a PLL in your design, you must import source constraints the first time the design is compiled.
Devices Affected:	ispMACH 5000VG
Issue:	When using the "Preserve" attribute for MACH devices, the report file does not show that the signals are preserved.
Solution:	The property is working correctly, but it is not reported in the report file.
Devices Affected:	All MACH devices

Issue:	The first line of VHDL code cannot be a commented line; it should be the library declaration.
Solution:	Use library declaration for the first line of VHDL code.
Devices Affected:	All
Issue:	The following constraints specified in the Schematic Editor will not work: PULL, SLOWRATE, OPENDRAIN, VOLTAGE, GROUP, RESERVE, CRIT, OUTDELAY.
Solution:	Use the Constraint Editor to specify the constraints.
Devices Affected:	ispLSI 1000/2000/8000
Issue:	Reserved pin assignments are not reported in the design summary section of the report file.
Solution:	None.
Devices Affected:	MACH 5
Issue:	When using PLLs in your design, prefit.exe will always generate a warning message regarding the removal of intermediate nodes associated with the PLL that are inserted by the synthesis tools.
Solution:	Ignore the warnings.
Devices Affected:	ispMACH 5000VG
Issue:	ispMACH 4A3/4A5, MACH 4/4A, and MACH 5/5LV devices support only ASCII format for USERCODE user constraint.
Solution:	None.
Devices Affected:	ispMACH 4A3/4A5, MACH 4/4A, and MACH 5/5LV

Issue:	You cannot set both the GLB clock (CLK1, CLK2) and the IOC clock (IOCLK0, IOCLK1) in the Constraint Editor, for all the ispLSI 1000 devices. For example, to use one clock "GLB_IOC" to clock a register in both the GLB and IOC, the setting would be GLB_IOC=CLK1,IOCLK0. See page 10 of the <i>1000EA Data Sheet</i> to understand the clock matrix and this limitation.
Solution:	You can set the clock in the ABEL source using the legacy ABEL attributes plsi PROPERTY 'CLK glb_io_clk clk1 ioclk0';
	There is no solution for the Verilog and VHDL because the attributes are not supported in the source.
Devices Affected:	ispLSI 1000/1000E/1000EA

ispVM Programming System Issues

Issue:	The ISC compiler might report a false verify failure when using the ISC BSDL files. This may be a false failure due the speed improvements made to TCK, TDI, TMS, and TDO for our faster devices.
Solution:	 Use the standard ispVM support, or; Slow down the TCK clock by selecting Projects > Project Setting, and select Advanced button. In the TCK Clock pulse width in microseconds box, enter a value of 3 or greater.
Devices Affected:	MACH 4/5

Issue:	The USERCODE support for ispLSI 8000, 8000V, 5000VA, 5000VE, 2000E, 2000VE, 2000VL, 1000EA, ispGDX-V/VA family of devices was changed in version 9.0.4. The order the 32-bit USERCODE is programmed into the device, shifted out, and displayed in the ispVM GUI was changed to match the MACH device support. For these devices, the order the USERCODE bits are displayed in the GUI and the order they are written in the SVF file will match the order they are contained in the JEDEC file. For example, if the JEDEC file contains the following U field: U000000010010010011010001011100111 or: UH01234567
	The USERCODE will be programmed into the device as 0x01234567, the GUI will display the USERCODE as "0x01234567", and the USERCODE will be written in the SVF file as: SDR 32 TDI (01234567);
	Note: Devices programmed using ispVM V9.0.3 software, or earlier, will fail verify on V9.0.4 since the order they are programmed into the device has been swapped. To correct this error, reprogram the devices using ispVM V9.0.4 or later. The ispVM 9.0.4 software will fix the problem, as will later versions.
	Note: Because of this change, these devices can no longer be cross verified with ispDCD. The ispDCD will report a verify failure on the Usercode.
Solution:	None
Devices Affected:	ispLSI 8000, 8000V, 5000VA, 5000VE, 2000E, 2000VE, 2000VL, 1000EA, ispGDX-V/VA
Issue:	When performing a SCAN CHAIN with ispVM, if an ID code is detected that is shared by multiple devices, ispVM will display a generic device name, and will give a warning.
Solution:	Select the correct device.
Devices Affected:	ispLSI 2032VE/VL, 2064VE(VL), 2064VE(VL)-44Pin, 2096VE(VL), 2128VE(VL), 2128VE(VL)-100Pin, and 2192VE(VL)

Online Help/Documentation Issues

Issue:	If you install, uninstall, and re-install ispLEVER to a different location on your hard drive, you may receive an error message when you attempt to start Help. This can be caused by conflicts between the new location of Help and its old .gid file. GID files (<i>help_file_name.gid</i>) are configuration files that are dynamically created by Windows when starting Help, and contain the last location of the Help file. If the GID file is out of sync with the Help file (for example the GID file was not deleted during the uninstall process), you will receive a message saying that the Help file cannot be found
Solution:	Search for and delete all files with the extension .gid on your hard drive. Windows will automatically create a new GID file for each help system on your computer when you start the help system.
Devices Affected:	All